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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,524	08/07/2001	Chun Wang	ATI.0001670	1770

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/923,524	Applicant(s) WANG ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12/02/2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-41 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-41 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed December 03, 2003 have been fully considered but they are not persuasive. In response to Applicant's arguments that reference Tomko (U.S. Patent No. 5,878,240) does not teach receiving configuration data, the examiner disagrees. As stated in previous Office Action, Tomko teaches the processing system as shown in Fig. 1, comprises a bus control configures a transfer bus and forwards a memory access command to the target memory such that the source processor can then access the target memory as well as its own memory (routing access requests). This configuration remains active until any of the processors requests a memory address outside of the current configuration or the processor associated with the target memory requests its own memory again. In response, the bus control again causes the transfer bus to be reconfigured (col. 2, lines 23-35). Thus, each of the memory controllers (A-C) receives configuration data from the bus control 24 of the processing system 16. Further, Tomko teaches the system 16 integrated in one circuit card (col. 3, lines 16-17).

As for Applicant's arguments that reference Murakami (U.S. Patent No. 6,330,036) does not teach a plurality of memory controllers, the examiner refers to Fig. 9, wherein the system includes enlarger/reducer units (310a, 310b, ..., 310n) (memory controllers) receiving decoded video signals 156 (a) – (n) (configuration data), and then synthesized in the screen overlay unit 302 and outputted to the monitor 332 as a synthesized signal 352. As a result, a plurality of pictures corresponding to respective channels are displayed on a monitor 332 (col. 10, lines 1-9). In addition, Murakami et al. teach a video decoder 106 in a digital video receiving apparatus as shown in Fig. 2, comprises a plurality of video decoders (202a, 202b, . . . 202n), wherein the

video stream 153 input to the video decoder 106 is divided into bit streams for each channel corresponding to programs using the stream identification signal 155 (col. 6, lines 20-22). Since Applicant does not specify "configuration data," the rejection is still based on the broadest reasonable interpretation.

In regard to Applicant's argument that reference McInnis et al. (U.S. Patent No. 6,189,064) does not teach the router to route data at each one of the plurality of first input ports to a respective output port of the first or second output port based upon the data stored in the storage module, the examiner refers to Figure 27 where the memory controllers are connected to the video FIFO 148 (a storage module). Details of the memory controllers are illustrated in Fig. 32, and cited in previous Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-3, 5-6, 8-21, and 23 are rejected under 35 U.S.C. 102(a) as being anticipated by Tomko (U.S. Patent No. 5,878,240).

Referring to claims 1-3, 21, and 23, as shown in Fig. 1, Tomko teaches a processing system integrated in one circuit card 16, which plugs into bus 14, comprises, according to the exemplary embodiment, three processors (clients), labeled as A, B, and C, and three sets of memories, memory A, memory B, and memory C, each associated with a respective processor, and each memory having a controller (memory controller A, memory controller B, and memory

controller C, respectively) that allow full-speed, burst-mode access by the processors (col. 3, lines 16-24, and 36-40). Tomko teaches the system further comprises a bus control (numeral 24, Fig. 1) configures a transfer bus and forwards a memory access command to the target memory such that the source processor can then access the target memory as well as its own memory (routing access requests). This configuration remains active until any of the processors requests a memory address outside of the current configuration or the processor associated with the target memory requests its own memory again. In response, the bus control again causes the transfer bus to be reconfigured (col. 2, lines 23-35).

In regard to claim 5, Tomko teaches bus control 24 provides a "round robin" arbitration system. That is, whichever processor used the bus for access to another's memory last is placed on the end of the priority queue the next time there is contention. Otherwise, the bus control 24 uses an alphabetical system (processor A, processor B, processor C, I/O-PC) to arbitrate among the four contenders (col. 5, lines 35-41).

In regard to claim 6, Tomko teaches processors A, B, and C each comprise Motorola Power PC-604 processors (col. 3, lines 24-26), and thus are of common type.

Referring to claims 8-10, as illustrated in Fig. 1, Tomko teaches bus control 24 monitors the signals on control leads 20A, 20B, and 20C for situations where a processor issues a transaction start signal with a memory address of a memory other than its own (col. 4, lines 61-64), and as shown in Fig. 1, these control leads 20A-20C route the requests from respective processors A-C to their respective memory controllers A-C.

In regard to claim 11, as shown in Fig. 2, Tomko teaches processing starts in the "normal", stable state 200 where each processor is granted access to its own memory. In this

state, processor A is granted access to memory A, processor B is granted access to memory B, and processor C is granted access to memory C. A transition event 202 occurs when one or more processors address a memory other than their own. This causes a transition to setup state 204 which is a transitory state. In the setup state, the bus control 24 decides which process will control the transfer bus by accessing its arbitration table. The bus grant signal is removed from the processor associated with the target memory. After any pending transaction between the processor associated with the target memory and the target memory is completed, as evidenced by issuance of an idle signal from the target memory controller, the source processor is connected to the target memory and a transaction start signal is provided by bus control 24 to the controller for the target memory (col. 6, lines 30-46).

Referring to claims 12-16, as cited above, Tomko teaches bus control 24 provides a "round robin" arbitration system. That is, whichever processor used the bus for access to another's memory last is placed on the end of the priority queue the next time there is contention (first arbitration scheme). Otherwise, the bus control 24 uses an alphabetical system (processor A, processor B, processor C, I/O-PC) to arbitrate among the four contenders (second arbitration scheme) (col. 5, lines 35-41).

In regard to claims 17 and 19, Tomko teaches one of the requesting processors is selected (according to the arbitration table) to be the next source processor. The arbitration table uses the previous values (an identifier) of the source (processor) register and the values of the request registers to determine the new source processor wherein the "winner" is awarded access to the transfer bus.

Referring to claims 18 and 20, as cited above, Tomko teaches assigning priority based on a certain arbitration scheme. Tomko further teaches when a processor wishes to access memory (either a read or write) it issues a transaction start signal and the memory address for the beginning of the transaction (within 9.5 nanoseconds after the rising edge of the clock pulse). The transaction start signal lasts only one clock pulse (15 nanoseconds). The rest of the control signals remain until the processor receives an "address acknowledge" signal from its memory controller (col. 3, lines 65-67, and col. 4, lines 1-5). Thus, the priority is assigned depending on an internal timer, and the number of requests from the processors depends on the data rate.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 24-32, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by MacInnis et al. (U.S. Patent No. 6,189,064).

Referring to claims 24-26, 29, and 32, as shown FIG. 32, MacInnis et al. teach a dual memory controller system services memory requests generated by a display engine 1118, a CPU 1120, a graphics accelerator 1124 and an input/output module 1126 (clients) are provided to a memory select block 1100 (a router). The memory select block 1100 preferably routes the memory requests to a first arbiter 1102 or to a second arbiter 1106 based on the address of the requested memory. The first arbiter 1102 sends memory requests to a first memory controller 1104 while the second arbiter 1106 sends memory requests to a second memory controller 1108.

The first and second memory controllers preferably provide first and second data received, respectively, from the first and second external SDRAMs to a device that requested the received data. The first and second arbiters handle requests from tasks with different priorities (col. 52, lines 64-67, and col. 53, lines 1-18). Thus, from the above clients, at least two clients, a CPU 1120 and graphics accelerator 1124 for example, are of common type when they process graphics.

In regard to claims 27 and 28, as shown in Fig. 36, MacInnis et al. teach a process of servicing memory requests with different priorities, from the highest to the lowest. A video window read request in step 1174 and a video capture write request in step 1176 have equal priorities (request of common type). Therefore, the video window read request and the video capture write request are placed in a round robin arbitration for two tasks (clients). The system in steps 1184, 1188 and 1190 places other lowest priority tasks such as a graphics accelerator read/write request, a DMA read/write request and a CPU write request, respectively, in this round robin arbitration with five clients (a second arbitration) (col. 57, lines 42-67).

In regard to claim 30, MacInnis et al. teach the first memory controller preferably sends address and control signals to a first external SDRAM and receives a first data from the first external SDRAM. The second memory controller preferably sends address and control signals to a second external SDRAM and receives a second data from the second external SDRAM (col. 53, lines 9-14).

Referring to claims 31 and 34, MacInnis et al. teach a FIFO in the graphics display path accepts raw graphics data as the raw graphics data is read from memory, at the full memory data rate using a clock of the memory controller (col. 15, lines 41-45).

6. Claims 1, 22, 35-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Murakami et al. (U.S. Patent No. 6,330,036).

Referring to claims 1, 22, 35-36, 38-41, with reference to Figs. 2 and 8, Murakami et al. teach a video decoder 106 in a digital video receiving apparatus as shown in Fig. 2, comprises a plurality of video decoders (202a, 202b, . . . 202n), wherein the video stream 153 input to the video decoder 106 is divided into bit streams for each channel corresponding to programs using the stream identification signal 155 (col. 6, lines 20-22). In operation, the HDTV signal inputted into the video decoder 106 is divided into each partial video signal corresponding to each partial picture based on the video stream 153, the clock signal 154 and the stream identification signal 155, and the respective divided partial video signal are sent to respective video decoders (202a, 202b, . . . 202n). The partial video decoders (203a, 203b, . . . 203n) in the respective video decoders (202a, 202b, . . . 202n) decode each partial video signal. If data from adjacent video decoders (202a, 202b, . . . 202n) are needed for decoding, respective video decoders (202a, 202b, . . . 202n) decode the signals using inter-video decoder connection lines (255a, 255b, . . . 255n) and memories (204a, 204b, . . . 204n), and output decoded signals (156a, 156b, . . . 156n). The decoded signals (156a, 156b, . . . 156n) outputted from the video decoder 106 are input to the display synthesizer 109 (col. 9, lines 30-50), as shown in Fig. 9, which includes enlarger/reducer units (310a, 310b, ..., 310n) (memory controllers). The respective decoded video signals (156a, 156b,...,156n) received from the video decoder 106 are input to the enlarger/reducer units (310a, 310b, . . . 310n) for each part (col. 10, lines 1-9).

In regard to claim 37, Murakami et al. teach the video decoder 106 decodes each video stream using the input clock signal 154 corresponding to the program and the stream

identification signal 155, and outputs decoded video signals (156a, 156b, ..., 156n) for each program as video output signals (col. 6, lines 4-8).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomko (U.S. Patent No. 5,878,240) in view of MacInnis et al. (U.S. Patent No. 6,189,064).

Referring to claims 4 and 7, as applied to claims 3 and 6 above, Tomko teaches all the limitations of claims 4 and 7, except for the device having a graphics controller, and the common client type include one of the group of two-dimensional graphics driver, three-dimensional graphics driver, and an audio driver.

However, as cited above, MacInnis et al. teach a memory controller system comprising a plurality of clients, and a method of routing requests from each of the clients to its respective memory controller, and the clients includes a display engine 1118, a CPU 1120, a graphics accelerator 1124. The graphics accelerator may perform graphics operations on three dimensional graphics images (col. 5, lines 62-64).

Therefore, it would have been obvious to one skilled in the art to utilize the teachings as taught by MacInnis et al. in combination with the method as taught by Tomko in order to handle memory request while processing graphics.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis et al. (U.S. Patent No. 6,189,064) in view of Murakami et al. (U.S. Patent No. 6,330,036).

Referring to claim 33, as applied to claim 24, MacInnis et al. teach all the limitations of claim 33, except that the first and second memory controller receive HDTV stream from the router.

However, as cited above, Murakami et al. teach a digital video receiving apparatus comprising a plurality of video decoders coupled to receive HDTV stream and output to respective memory controllers.

Therefore, it would have been obvious to one skilled in the art to utilize the teachings as taught by Murakami et al. in combination with the teachings as taught by MacInnis et al. in order to decode different types of TV pictures simultaneously (col. 2, lines 20-22).

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

02/02/2004

Matthew C. Bella

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